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# Clock Related Flip-Flop with Sleepy Transistor Merging For Power Saving

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**Abstract:** The need for low-power design is also becoming a major issue in high-performance digital systems such as microprocessors, digital signal processors (DSPs) and other applications. The dominant factor of power dissipation is caused by switching activity. As low power circuits are most popular now days as the scaling increase the leakage power in the circuit also increases rapidly and so for removing these kinds of leakages and to provide a better power efficiency different types of power gating techniques are used. The different types of power gated circuits using low power VLSI design techniques are analysed and comparison results are displayed. As compared with conventional flip-flops, the flip-flop reduces power dissipation by 75% at 0% data activity and the power reduction ratio is the highest among flip-flops that have been reported so far. The simulations were done using Microwind Layout Editor and DSCH software.

**Keywords:** Flip-flops, Low-power, VLSI, Transistor.

## I. INTRODUCTION

The mobile market keeps on expanding. In addition to the conventional mobile phone, digital camera, and tablet PC, development of various kinds of wearable information equipment or healthcare associated equipment has newly prospered in recent years. In those kinds of battery-working equipment, reduction of power is a very important issue and demand for power reduction in LSI is increasing. Based on such background, various kinds of circuit technique have already been proposed. Generally in LSI, more than half of the power is dissipated in random logic of which half of the power is dissipated by flip-flops (FFs). During the past dozen years, several low-power FFs have been rushed into development. However, in actual chip design, the conventional FF is still used most often as a preferred FF because of its well-balanced power and performance.

The scaling of process technologies to nanometres scheme has resulted in a rapid increase in leakage power dissipation. Since, it has become extremely important to develop design techniques to reduce static power dissipation during periods of inactivity. The power reduction should be achieved without trading-off performance which makes it harder to reduce leakage during normal (runtime) operation. On the other hand, there are several techniques for reducing leakage power.

Power gating is one of the well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground). This device is turned-off in the sleep mode to cut-off the leakage path.

## II. POWER REDUCTION IN FLIP-FLOP

A. Topologically compressed flip-flop

The power of the Flip-flop is mostly dissipated in the operation of clock-related transistors and hence the clock signals uses more power rather than other signals.

Before analyzing the operation of the circuit, the combinational circuit of the D Flip-flop is shown in the Fig.1.

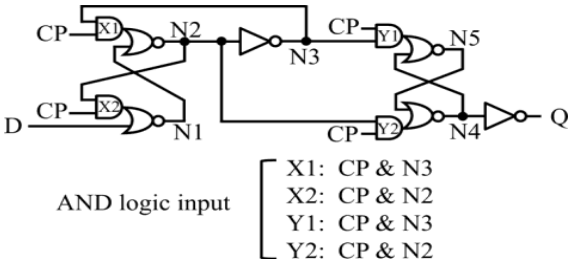


Fig. 1 Schematic Diagram of D Flip-Flop

As the first step, a circuit with two or more logically equivalent AND or OR logic parts which have the same input signal combination, especially including clock signal as the input signals. Then, merge those parts in transistor level as second step. This is well-known Reset-Set (RS) type, but the master-latch is an asymmetrical single data-input type. The feature of this circuit is that has two sets of logically equivalent input AND logic, X1 and Y1, and X2 and Y2. Fig. 2 shows transistor-level schematic of Fig.1.

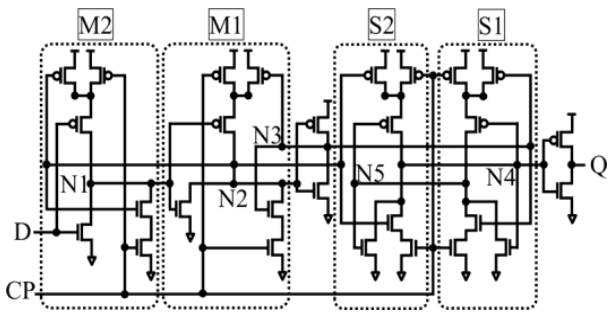


Fig. 2 Transistor Level Schematic of Fig. 1

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Based on this schematic, logically equivalent transistors are merged as follows. For the PMOS side, two transistor pairs in M1 and S1 blocks in Fig. 2 can be shared. When either N3 or CP is Low, the shared common node becomes VDD voltage level, or N2 and N5 nodes are controlled by PMOS transistors gated N1 and N4 individually. When both N3 and CP are High, both N2 and N5 nodes are pulled down to VSS by NMOS transistors gated N3 and CP. As well as M1 and S1 blocks, two PMOS transistor pairs in M2 and S2 blocks are shared.

This reduction method is called Topological Compression (TC) method. The Flip-flop, TC-Method applied, is called Topologically-Compressed Flip-Flop (TCFF). The Fig.3 shows the Transistor level schematic of topologically-compressed Flip-flop. In Fig. 3, when CP is low, the PMOS transistor connected to CP turns on and the master latch becomes the data input mode. Both VD1 and VD2 are pulled up to power-supply level, and the input data from D is stored in the master latch. When CP is high, the PMOS transistor connected to CP turns off, the NMOS transistor connected to CP turns on, and the slave latch becomes the data output mode. From the Fig. 2, the total transistor count is 28 and after merging the clock related transistors the total transistor count is reduced to 21 transistors as shown in Fig. 3.

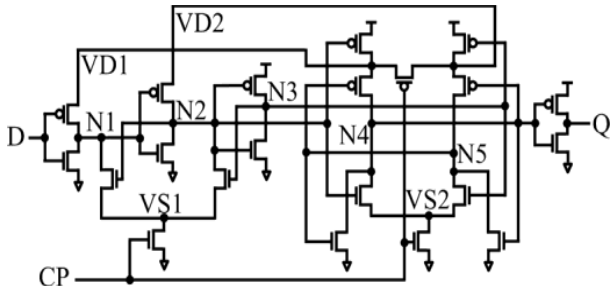


Fig. 3 Transistor Level Schematic of Topologically Compressed Flip-flop (TCFF)

In this operation, all nodes are fully static and full-swing. The current from the power supply does not flow into the master and the slave latch simultaneously because the master latch and the slave latch become active alternately. Therefore, timing degradation is small on cell performance even though many transistors are shared and so it is advisable to reduce the leakage power consumed by each transistor [13]. Let us summarize the analysis of low power Flip-flop, since this technique make use of reducing the clock related transistor count by merging process and therefore the power consumed by the transistor is minimized[4]. So far the leakage power is increased. So, to reduce the leakage power the sleep methods are used and hence the power consumed by the Flip-flops is reduced drastically.

B. Topologically compressed flip-flop using sleepy method

Different methods exist for leakage power reduction. Whenever the circuits are working we have to make the sleep transistors ON.

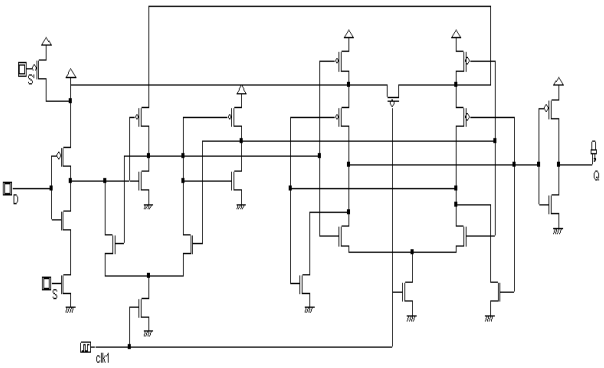

Fig. 4 TCFF Using Sleep method

A variation of the sleep approach is also known as the zigzag approach as shown in the Fig. 4, decreases wake-up overhead caused by sleep transistors.

Another method called Dual sleep approach as shown in the Fig. 5 uses the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. Hence, the dual sleep portion can be made common to all logic circuitry; less number of transistors is needed to apply a certain logic circuit.

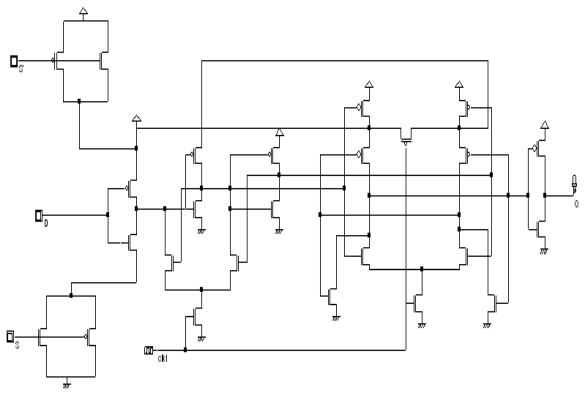

Fig. 5 TCFF Using Dual Sleep Method

Another technique is dual stack approach, in sleep mode; the sleep transistors are off, i.e. transistor N1 and P1 are off. We do so by making S=0 and hence S'=1. So, that the 4 transistors P2, P3 and N2, N3 are connected to the main circuit with power rail.

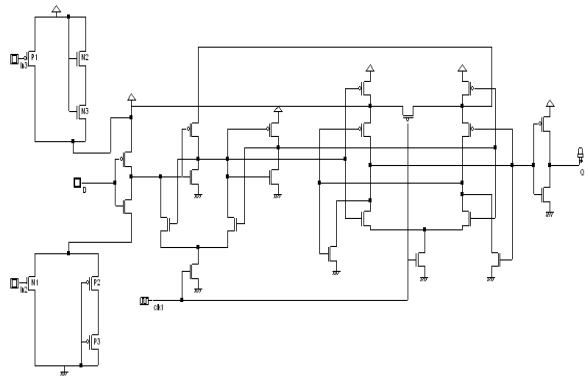

Fig. 6 TCFF Using Dual Stack Method


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Hence, we use 2 PMOS in the pull down network and 2 NMOS in the pull-up network. The advantage is that PMOS degrades the low logic level while NMOS degrades the high logic level. Due to the body effect, they further decrease the voltage level. So, that the pass transistors decreases the voltage applied across the main circuit. In practice, the static power is proportional to the voltage applied, with the reduced voltage the power is decreased but we get the advantage of state retention.

Another merit is got during off mode if we increase the threshold voltage of N2, N3 and P2, P3 transistors. The transistors are held in reverse body bias and their threshold is high. Since, high threshold voltage causes low leakage power and hence low leakage current. By using minimum size transistors, i.e. aspect ratio of 1, we get low leakage power due to low leakage current and as a result of stacking; P2 and N2 have less drain voltage. Hence, the DIBL effect is less for them and they cause high barrier for leakage current. In the active mode i.e. S=1 and S'=0, both the sleep transistors (N1 and P1) and the parallel transistors (N2, N3 and P2, P3) are on. They work as transmission gate and the power connection is again established in uncorrupted way and the dynamic power is reduced.

The power gated sleep circuit has three modes of operations
1. Active mode
2. Standby mode
3. Sleep to active mode transition

In active mode, the sleep Signal S of the transistor is held at logic' 1 ' and both the sleep transistors M1 and M2 (En and En-Bar Transistors from the bottom side) remain ON. Here both the transistors offer very low resistance and virtual ground (VGND) node potential is pulled down to the ground potential. There are huge benefits of combining stacked sleep transistors. Firstly, the magnitude of power supply fluctuations sleep mode during mode transitions will be reduced because these transitions are gradual. Secondly, while conventional power gating uses a high-threshold device as a sleep transistor to minimize leakage and a stacked sleep structures can achieve the same effect with a normal threshold device.

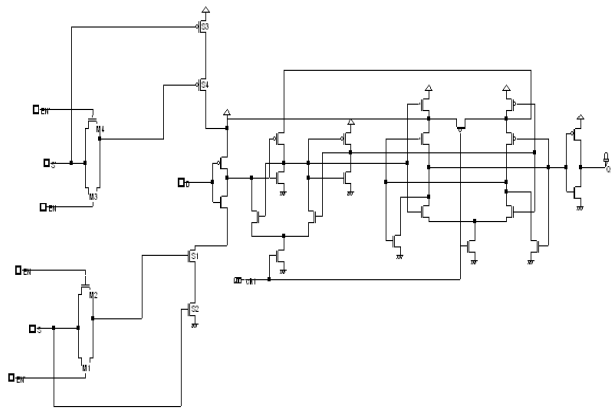

Fig.7 TCFF Using Power Gated Sleep Method

In stand-by mode, the sleep signal of the transistor is held at logic'1' and both the sleep transistors S1 and S2 (NMOS Transistors used for sleep Purpose from the Bottom of the circuit) remain ON and control the transistors M1 & M2 is OFF by giving logic'0'.Hence, the leakage current is reduced by the stacking effect, turning S1 and S2 sleep transistors OFF and vice versa for the header switch. This design gives major contribution in sleep to active mode in terms of peak of sleep mode compared to stacking power gating. Sleep mode occurs when the circuit is going from sleep to active and vice versa. In first stage the sleep transistor (S1) working as diode by turning on the control transistor M1 which is connected across the drain and gate of the sleep transistor (S1). Due to this the drain to source current of the sleep transistor S1 drops in a rectilinear manner. This reduces the voltage fluctuation on the ground and power net and it also reduces the circuit wake-up time. So in sleep to active transition mode, we are turning ON transistor S1 initially after a small duration, S2 will be turned ON to reduce the GBN. In the second stage control transistor is off that sleep transistor works normally. During sleep to active mode transition, the transistors S1 and S2 is turned ON and after a small duration of time. The logic circuit is isolated from the ground for a short duration as the transistor S2 is turned OFF. During this duration, the GBN is greatly reduced by controlling the intermediate node voltage VGND2 and operating the transistor S2 in triode region. Placing the proper amount of delay, Leakage current is decreased by stacking effect which turns both S1 and S2 sleep transistors OFF. This boosts the intermediate node voltage VGND2 to positive values due to small drain current. Positive potential at intermediate node has the following effects:

- Gate to source voltage of S1 (Vgs1) becomes almost negative.
- Negative body-to-source potential (Vdsl) of S1 decreases thus it results in less drain induced barrier lowering.
- Drain-to-source potential (Vds2) of S2 is less compared to S1, hence most of the voltage drops across the S1 in sleep mode.

This probably reduces the drain barrier lowering. Hence the leakage power is reduced in the circuit.

## III. RESULT AND DISCUSSIONS

The simulation results for the Flip-flop are obtained from Microwind tool. The input to each of flip-flop includes clock input, d input and q output. The circuits are drawn in Digital schematic editor (DSCH) and the corresponding waveforms and verilog codes are generated. The generated verilog codes are compiled in nanoLambda in which appropriate CMOS Layout is generated and the power results are obtained.
The Fig. 8, Fig. 9, Fig. 10, Fig. 11 shows the waveform of TCFF using Sleep method, TCFF using Dual Sleep method, TCFF using Dual Stack method, TCFF using Power Gated Sleep method respectively. The Fig. 12 shows the power result of TCFF using Power Gated Sleep method.


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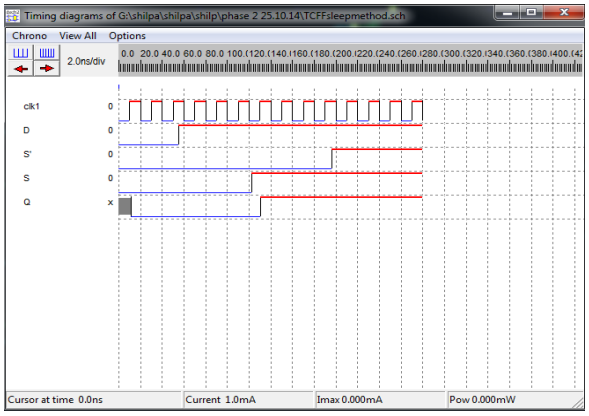


Fig. 8 Waveform of TCFF Using Sleep Method

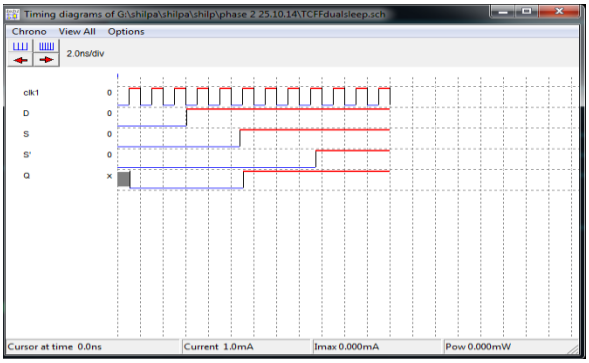


Fig. 9 Waveform of TCFF Using Dual Sleep Method

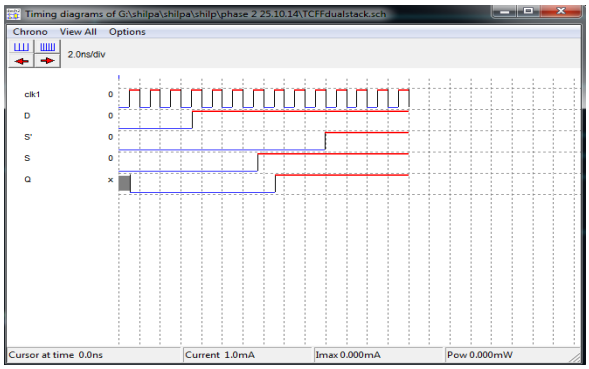


Fig. 10 Waveform of TCFF Using Dual Stack Method

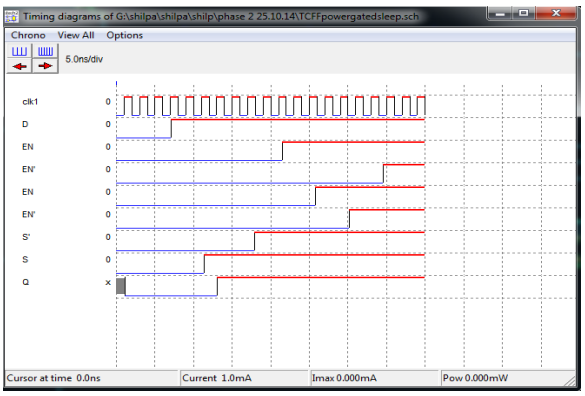


Fig. 11 Waveform of TCFF Using Power Gated Sleep Method

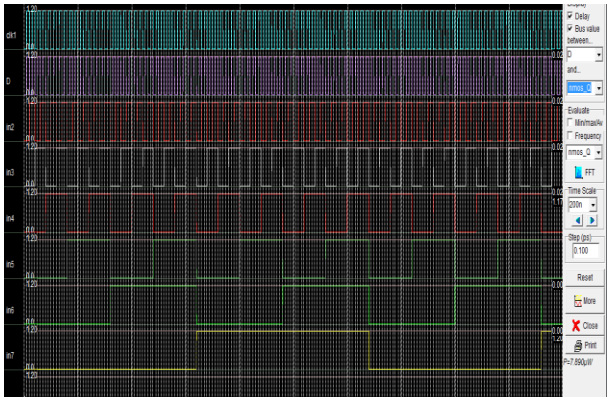

Fig. 12 Power Result of TCFF Using Power Gated Sleep Method

## IV. POWER COMPARISON

We compare the various TCFF Flip-flop with sleep transistor techniques. Thus,we compare various design approaches in terms of power consumption as shown below.

TABLE I POWER COMPARISON OF EXISTING AND PROPOSED METHODS

| Circuit Technique | Power Consumption(µw) |
|---|---|
| TCFF | 29.469 |
| TCFF Using Sleep Method | 11.339 |
| TCFF Using Dual Sleep Method | 15.359 |
| TCFF Using Dual Stack Method | 15.015 |
| TCFF Using Power Gated Sleep Method | 7.216 |

Table I shows power comparison of existing and proposed methods. The proposed power gated sleep method is 70% power efficient than the existing low-power flip-flops.

## V. CONCLUSION

In nanometer scale CMOS technology design, sub threshold leakage power consumption is a great challenge. Whereas previous approaches are effective in some ways, no ideal solution for reducing leakage power consumption is unknown. Therefore, the designers choose techniques based upon technology and design criteria. This paper presents a novel circuit structures which is a new remedy for designer in terms of power products. The power gated sleep method shows the least power product among all the methods. Therefore, the power gated sleep method provides new ways to designers who require ultra-low leakage power consumption with much less speed power product. Especially it shows nearly 50-60% of power than the existing methods. So, it can be used for future integrated circuits for power Efficiency. Applying to an experimental chip design with 90nm CMOS technology, 98% of the conventional flip-flops are replaced by this method. In a whole chip, 17% power reduction is

estimated with little overhead of area and timing performance. The simulation results proved that the proposed architecture is well suited for modern high performance designs.

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